QP CODE : 71248

LINEAR INTEGRATED CIRCUITS SOLUTION

(CBCGS SEM – 4 DEC 2019)

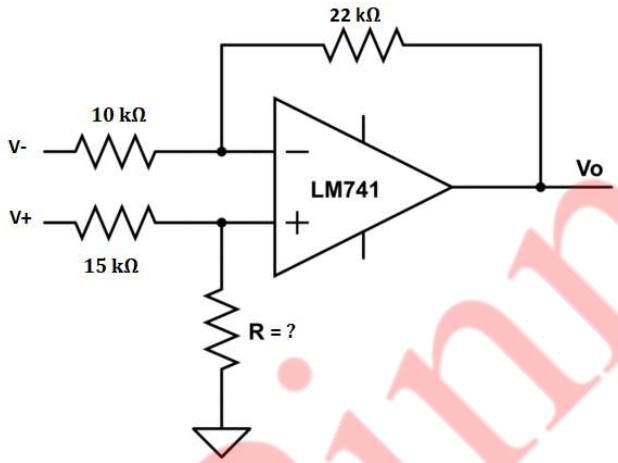
BRANCH – ELECTRONICS AND TELECOMMUNICATION

Q.1 Attempt the questions.

a) In the circuit given in Fig 1(a) if the voltage V+ and V- are to be amplified by the same factor, the value of R should be _____. (01)

i)3.3k Ω ii)33k Ω iii)330 Ω iv) None of these.

Justify. (04)



SOLUTION:

ii) 33 kΩ

The circuit above represents a subtractor circuit.

If R_F=22kΩ, R_1=10kΩ, R_2=15kΩ

Then, $\frac{R_F}{R_1} = \frac{R}{R_2}$ since input at both the terminals are to be amplified with same gain.

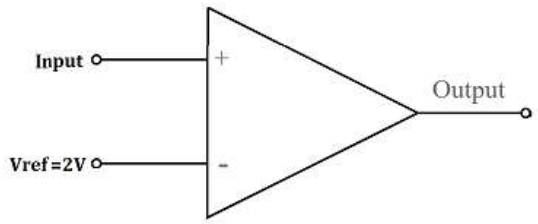
$$\frac{22 \times 10^3}{10 \times 10^3} = \frac{R}{15 \times 10^3}$$

R= 33 kΩ

b) If the input to the ideal comparator shown in Fig 1(b) is a sinusoidal signal of 8 volt peak to peak without any DC component, then the duty cycle is of the output comparator is _____. (01)

i)33.33% ii)25% iii)20% iv) None of these.

Justify. (04)



SOLUTION:

i) 33.33%

The above circuit acts as an open loop non-inverting comparator with an input of 8V peak to peak.

Hence, V_m=4 V and V_{REF}=2V.

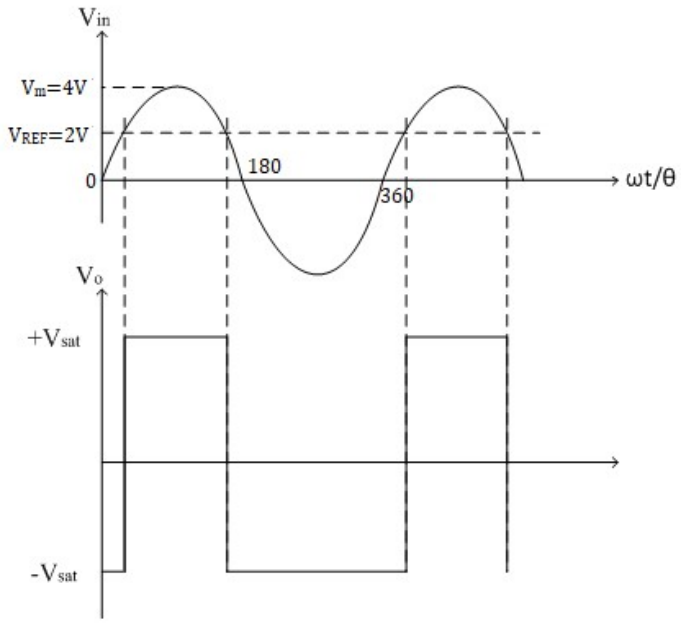
To find the duty cycle we need to know the on time (T_{ON}) and off time (T_{OFF}) of the circuit above which can be obtained from input output waveform.

This waveform can be plotted by non-inverting op-amp properties as follows

When, $V_{in} > V_{REF}$, $V_o = +V_{SAT}$

$V_{in} < V_{REF}$, $V_o = -V_{SAT}$

Hence the waveform is



From the output waveforms shown above, input signal crosses the reference point of 2V at two points in the positive half cycle of input signal. Therefore at the two crossing points we can have the equation-

$4\sin\Theta=2$

$\Theta=\sin^{-1}(\frac{2}{4})$

$\Theta= 30^{\circ}$

Thus at θ = 30°, input signal crosses the reference point. Since there are two reference points in the positive half cycle of input signal and both are symmetric from both the ends. So we get two angles corresponding to two crossings as follows,

$\Theta_1 = 30^{\circ}-0^{\circ}$ and $\Theta_2=180^{\circ} - 30^{\circ}$

$\Theta_1=30^{\circ}$ and $\Theta_2=150^{\circ}$

Thus between θ1 = 30° to θ2 = 150° output voltage is high (+Vsat). The complete cycle of input signal corresponds to θ = 360°. Thus the duty cycle of the output square wave can be represented as follows,

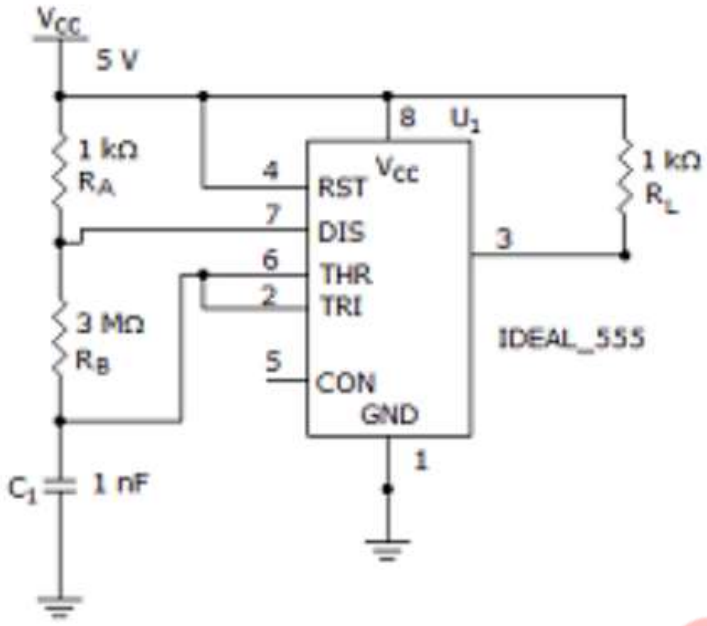
$$\text{Duty cycle} = D = \frac{T_{ON}}{T_{ON}+T_{OFF}} = \frac{150^{\circ}-30^{\circ}}{360^{\circ}} = \frac{120^{\circ}}{360^{\circ}} = \frac{1}{3}$$

D= 33.33%

c) What is the frequency of IC 555 astable multivibrator shown in Fig 1(c)? (01)

i) 241 Hz ii) 178 Hz iii)78 Hz iv) 8 Hz.

Justify. (04)



SOLUTION:

i) 241 Hz

Here $R_A=10^3\ \Omega$, $R_B=3\times10^6\Omega$ and $C=10^{-9}$

Since this is an astable multivibrator frequency is given by

$$f=\frac{1}{T}=\frac{1}{0.69(R_A+2R_B)C}=\frac{1}{0.69((10^3)+2(3\times10^6))\times10^{-9}}$$

f = 241 Hz

d) An amplifier using OPAMP with slew rate SR=1 V/µs has a gain of 40 dB. If this amplifier has to amplify sinusoidal signal of 20 KHz faithfully without any slew rate induced distortion, then the input signal must not exceed _____. (01)

i)795 mV ii)395 mV iii)79.5 mV iv) 39.5 mV

Justify. (04)

SOLUTION:

ii) 395 mV

Here SR= 1 V/µs = 10^6 V/s

Gain A_{VF}=40

f=20 kHz = 20×10^3 Hz

Since, slew rate = $\frac{dVo}{dT}\Big| max$

We need to find V_o

$V_o = A_{VF} \times V_m \sin(\omega t)$

$= 40 \times V_m \times \sin(2\times\pi\times f\times t)$

$= 40 \times V_m \times \sin(2\times\pi\times 20\times 10^3\times t)$

$\frac{dVo}{dT} = Vm \times 40 \times 2 \times \pi \times 20 \times 10^3 \times \cos(2\times\pi\times 20\times 10^3\times t)$

For $\frac{dVo}{dT}$ to be maximum i.e. slew rate cos term should be 1.

Therefore, $\frac{dVo}{dT}\Big| max = Vm \times 40 \times 2 \times \pi \times 20 \times 10^3$

$10^6 = Vm \times 40 \times 2 \times \pi \times 20 \times 10^3$

$V_m = \frac{10^6}{40\times 2\times\pi\times 20\times 10^3}$

V_m=198.94mV

This is maximum amplitude, hence the peak to peak voltage becomes

$V_{p\text{-}p}=2\times V_m$

$V_{p\text{-}p}$= 397.88mV.

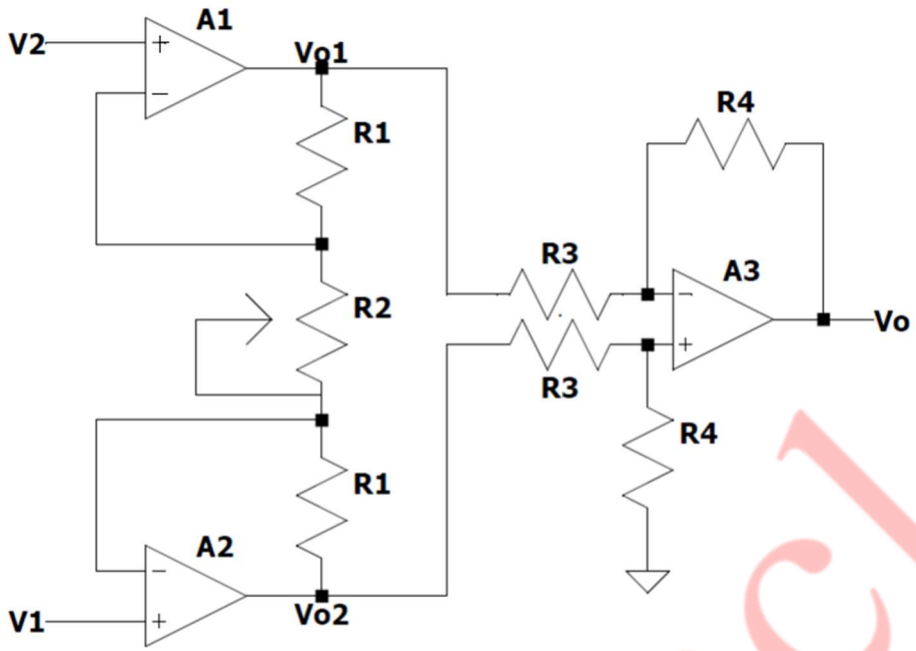
Hence the input signal must not exceed 395mV.

Q.2.

a) Sketch the implementation of an instrumentation amplifier using three op-amps and explain its operation. (10)

SOLUTION:

An instrumentation amplifier can be implemented using 3 op-amps as shown in the figure below.



Consider 3 op-amps A1, A2 and A3 where A1 and A2 act as non-inverting amplifier such that their inverting terminal (-) is connected to resistor R2 instead of ground.

The input impedance of all the op-amps (A1, A2 and A3) is assumed to be infinite, the currents flowing would be zero. Hence the current flowing through the resistors R1, R2 and R3 is same i.e. 'I'.

Using the concept of virtual short we can obtain the voltages at nodes A and B as follows

$V_A = V_2$ and $V_B = V_1$

Hence the expression for current I is,

$$I = \frac{V_A - V_B}{R_2} = \frac{V_2 - V_1}{R_2}$$

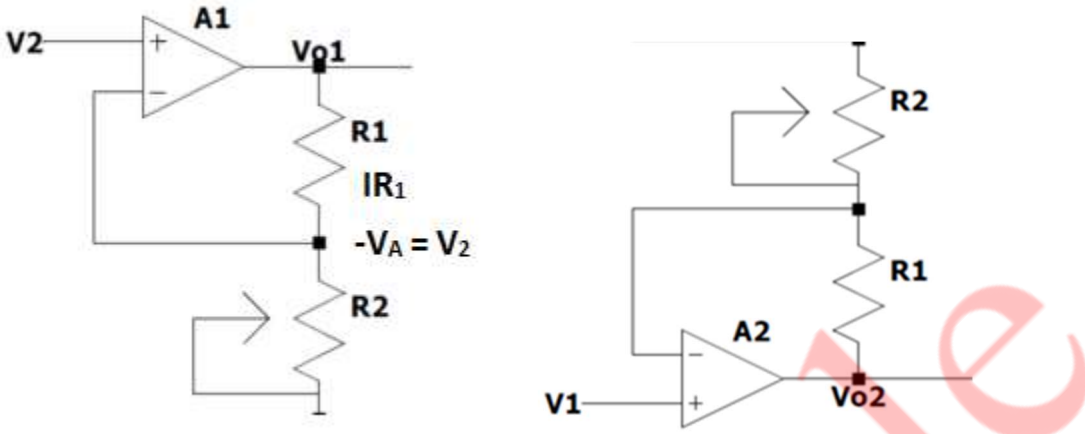
The output voltage of op-amp 2 (A2) is given by

$$V_{o2} = V_A + IR_1 = V_2 + IR_1$$

$$= V_2 + \left(\frac{V_2 - V_1}{R_2}\right)R_1$$

$$= \frac{V_2R_2 + V_2R_1 - V_1R_1}{R_2}$$

$$= \frac{(R_1 + R_2)V_2 - R_1V_1}{R_2}$$



The output voltage of OP-AMP1 is given by

$$V_{01} = V_B - IR_1$$

$$= V_1 - IR_1$$

$$= V_1 - \frac{V2 - V1}{R2} \times R_1$$

$$= \frac{V1R2 - V2R1 - V1R1}{R2}$$

$$= \frac{(R1 + R2)V1 - R1V2}{R2}$$

Hence the output of the first stage is given by

$$V_{02} - V_{01} = \frac{(R1 + R2)V2 - R1V1}{R2} - \frac{(R1 + R2)V1 - R1V2}{R2}$$

$$= \frac{(R1 + R2)(V2 - V1) + R1(V2 - V1)}{R2}$$

$$= \frac{(2R1 + R2)(V2 - V1)}{R1}$$

$$V_{02} - V_{01} = \left[1 + \frac{2R1}{R2}\right](V2 - V1)$$

Therefore, the gain of the first state is given by

$$A_{V1} = \frac{(V02 - V01)}{(V2 - V1)} = 1 + \frac{2R1}{R2}$$

The second stage is a difference amplifier with a gain of

$$A_{V2} = \frac{R4}{R3}$$

Therefore, the overall gain A_V of the three OP-AMP instrumentation amplifier is given by,

$$A_V = A_{V1} \times A_{V2}$$

$$\therefore \quad A_V = \left[1 + \frac{2R1}{R2}\right] \times \frac{R4}{R3}$$

Hence by using a variable resistor R_2 the overall gain can be easily and linearly varied.

The output voltage is then given by,

$$V_0 = A_V \times (V_1 - V_2)$$

The triple OP-AMP instrumentation amplifier is available in IC form. For example, ICAD522 or INA 101. These devices will contain all the components except the variable resistance R_2 shown in the figure above.

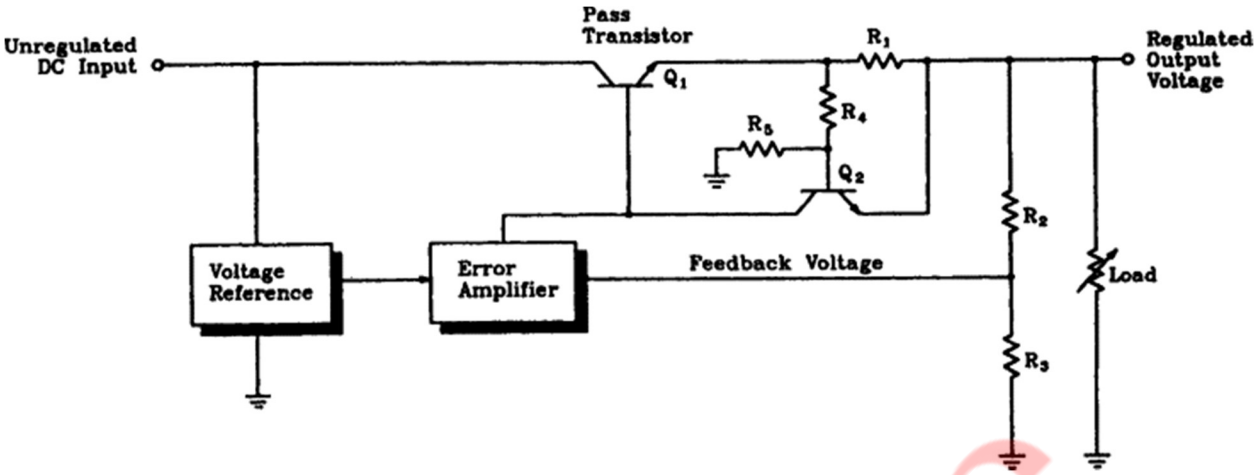
b) Compare Ideal and Practical op-amp. **(5)**

SOLUTION:

Sr.No.	Characteristics	Practical op-amp value	Ideal op-amp value
1	Input Resistance (R_i)	2 MΩ	Infinite
2	Output Resistance (R_o)	75 Ω	0
3	Voltage gain (A_V)	2×10^5	Infinite
4	Bandwidth B.W.	1 MHz	Infinite
5	CMRR	90 dB	Infinite
6	Slew rate (S)	0.5 V/µs	Infinite
7	Input offset voltage (V_{ios})	2 mV	0
8	PSRR	150 µV/V	0
9	Input bias current (I_B)	50 nA	0
10	Input offset current (I_{ios})	6 nA	0

c) Explain current foldback protection in voltage regualtors. (5)

SOLUTION:

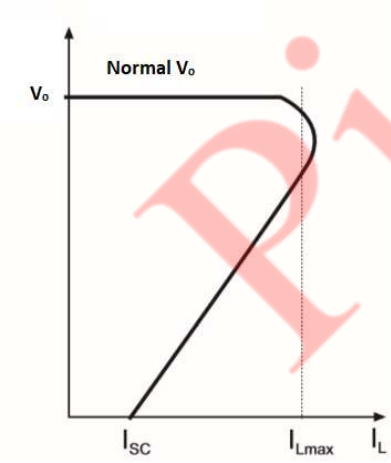


The circuit above shows a simplified circuit schematic of a discrete voltage regulator with foldback current limiting technique, which actually decreases the output current while operating in overload conditions.

The advantage of foldback current limiting is that it reduces the power dissipation taking place in the series pass transistor Q_1 under the short circuit condition as compared to power dissipation taking place in short circuit current protection.

As seen in the schematic above R_3 and R_4 are added to the short circuit protection.

Transfer characteristics of foldback current limiting circuit is as shown below



Q.3.

a) Design a Schmitt trigger circuit to convert 5V, 1 kHz sinusoidal signal to square wave using IC 741, V_{UT}=0.8V V_{LT}=-0.8V and $\pm V_{SAT}$ = ±11V. Draw its transfer characteristics, input and output waveforms.

SOLUTION:

Data:

$+V_{SAT} = +11V$, $-V_{SAT} = -11V$, $V_{UT}=0.8V$, $V_{LT}= -0.8V$, $V_{in} = 5V$

$f = 1\ kHz = 10^3\ Hz$ $\therefore T=\frac{1}{f} = \frac{1}{1000} = 1ms.$

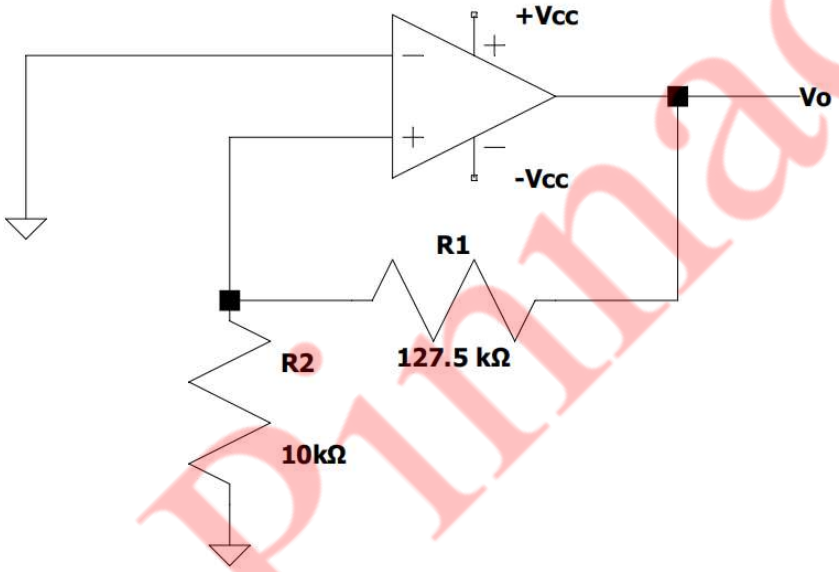
Let us assume $R_2 = 10k\Omega$

$\therefore V_{UT} = \frac{R_2}{R_1+R_2} \times V_{SAT}$

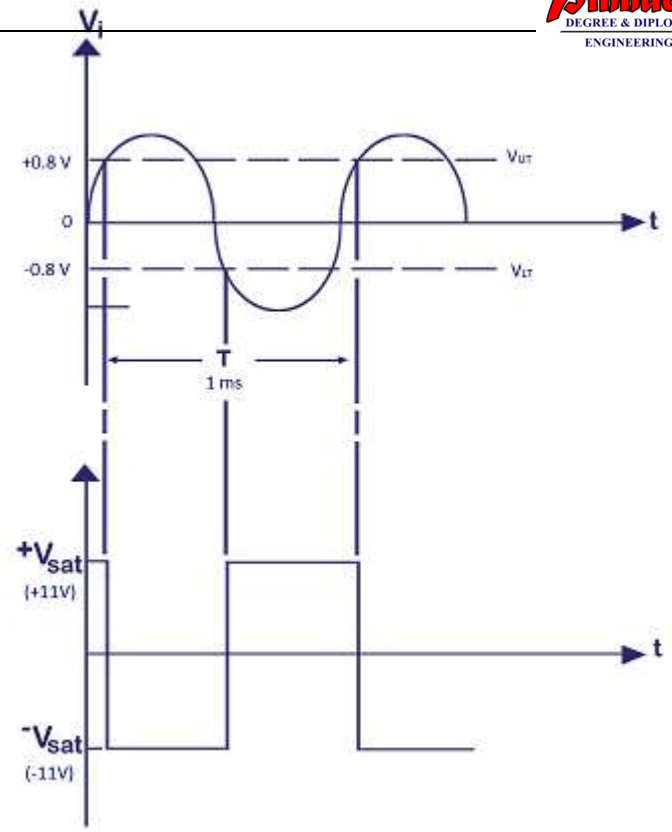
$\therefore 0.8 = \frac{10\times10^3}{R_1+1\ \times10^3} \times 11$

$R_1 = 127.5\ k\Omega$

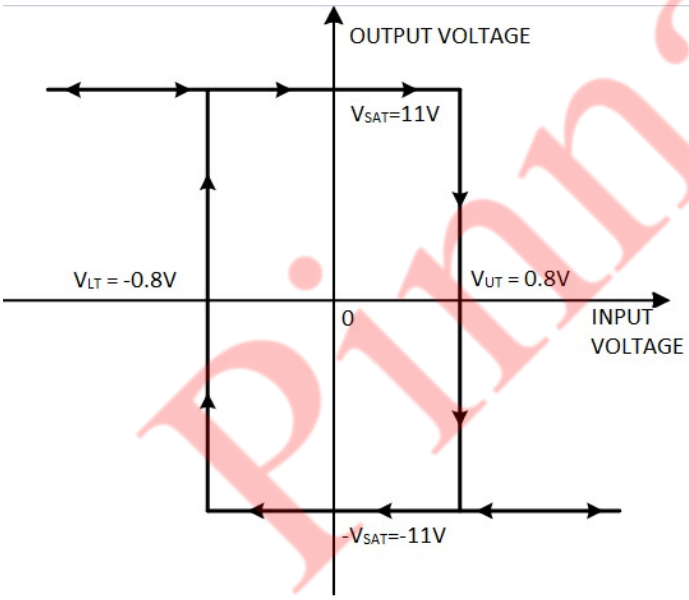
With this values of R_1 and R_2 the desired inverting Schmitt trigger can be obtained.



The waveform of input and output can be given as follow



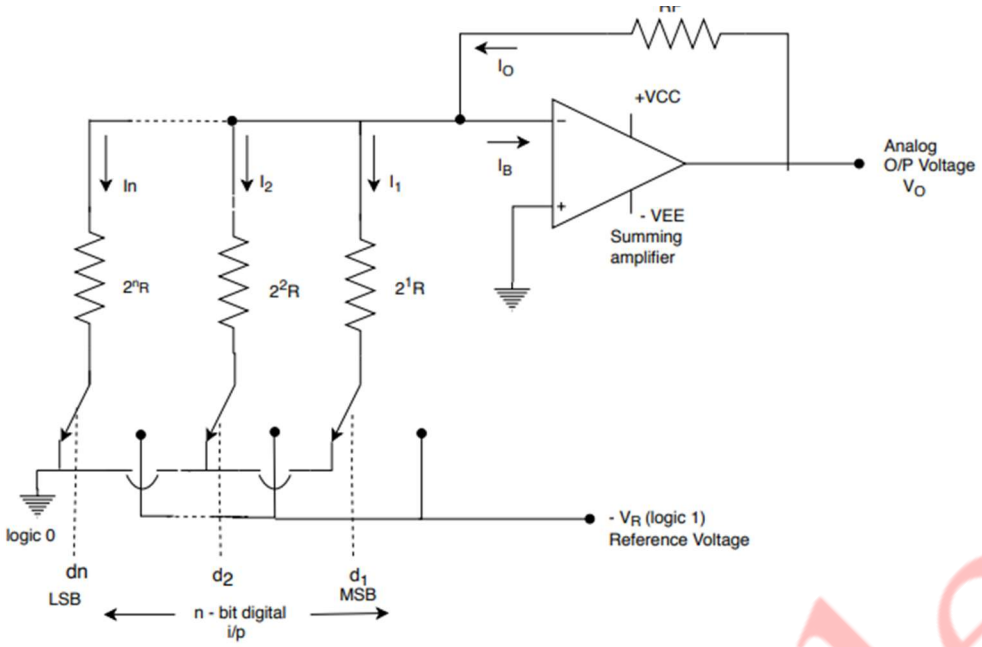
Transfer characteristics of above Schmitt trigger is



b) With the help of circuit diagram, derive the expression of output analog voltage for a weighted resistor DAC. (10)

SOLUTION:

The circuit diagram of binary weighted resistor type DAC is as shown below



This consists of 'n' binary weighted resistors and 'n' SPTD (Single Pole Double Throw) switches, whose position of moving arm is controlled by value of binary input applied to it.

Let the n bit digital input word to the DAC be d_1, d_2, d_3, …. d_n with d_1 as MSB (most significant bit) and d_n as LSB (least significant bit).

Let R_F be the feedback resistor and I_o be the output current. Let the op-amp be an ideal op-amp so that the current flowing into its terminals is zero due to its infinite input resistance.

Assuming the op-amp to be ideal , the output current I_o can be expressed as sum of individual currents through the weighted resistors (current going into op-amp is zero).

$I_o = I_1 + I_2 + ... + I_n$

$$\therefore I_o = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \cdots + \frac{V_R}{2^n R} d_n$$

Here $d_1, d_2, \ldots, d_n$ can have a value of '0' or '1'.

$$I_o = \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}) \qquad \text{(eqn. 1)}$$

The ouput voltage is given by

$V_o = I_o R_F$

$$V_o = V_R\frac{R_F}{R}(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$$

This is the required expression for output analog voltage. (eqn. 2)

From eqn. 1 and eqn.2 we can conclude that,

K=$\frac{R_F}{R}$ and $V_{FS} = V_R$.

So if $R_F = R$ and K=1

$$V_o = V_R(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$$

By substituting values of d_1, d2, d_3, …. d_n in above equation or eqn. 2 value of corresponding analog output voltage V_o can be obtained.

Q.4.

a) Design an IC 555 astable multivibrator for an output frequency 1 kHz and a duty cycle of 60%. (10)

SOLUTION:

Data:

Output frequency f_o = 1kHz = 10^3 Hz

Duty cycle D= 0.60

Let us assume C = 0.01µF

$$f_o = \frac{1.44}{(R_A + 2R_B)C}$$

$$\therefore R_A + 2R_B = \frac{1.44}{f_o \times C} = \frac{1.44}{10^3 \times 0.01 \times 10^{-6}}$$

$R_A + 2R_B = 144000$ ….(1)

Now, Duty cycle D = $\frac{R_A + R_B}{R_A + 2R_B}$

$0.6 = \frac{R_A + R_B}{144000}$ from equation (1)

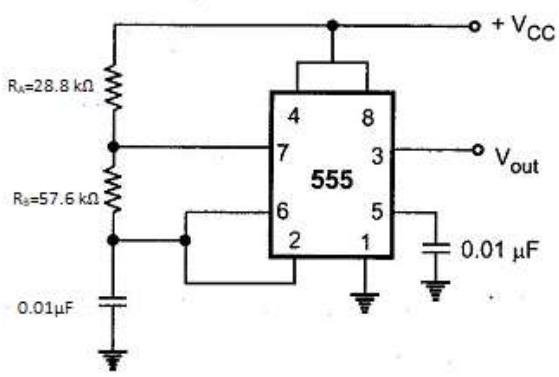
$R_A + R_B = 86400$ ....(2)

On solving equation (1) and (2)

$R_A = 28.8\ k\Omega$

$R_B = 57.6\ k\Omega$

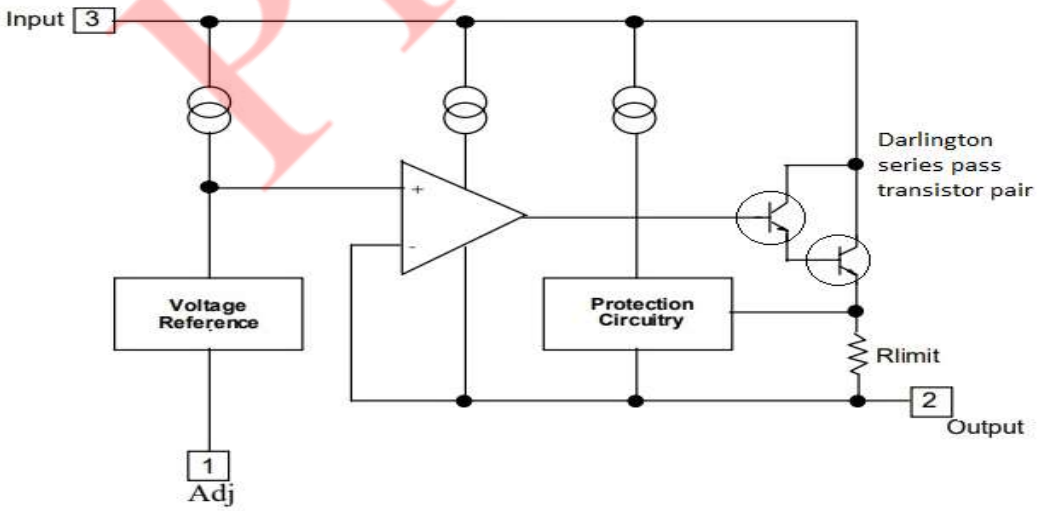
The circuit diagram of astable multivibrator as per above parameters is as given below



b) With the help of a functional block diagram explain the working of voltage regulator LM 317 to give an output voltage variable from 6V to 12V to handle maximum load current of 500mA. (10)

SOLUTION:

1. Functional block diagram of positive adjustable voltage regulator LM 317 is as shown below



2. The functional block diagram above shows that LM 317 is a series regulator and a Darlington pair acts as a series pass element.

3. The output voltage is compared with the internally generated voltage reference to produce an error voltage which drives the Darlington transistor to regulate the output voltage.

4. R_{LIMIT} is an internal sensing resistance. The voltage across it is proportional to load current. This voltage is applied to the internal protection circuitry.

5. If the load current exceeds beyond its maximum value, the Darlington pair will be automatically turned off to protect the IC.

6. LM 317 is monolithic IC voltage regulator with an adjustable output voltage which can supply more than 1.5A current to the load. Its output voltage is adjustable over a range of 1.2V to 37V.

7. It employs the internal current limiting and thermal shutdown and safe area compensation.

Data: V_o = 6V to 12V

I_L(max) = 500mA

Let us assume maximum value of I_{ADJ} = 100µA and let R_1 = 240Ω.

1. Calculate minimum and maximum values of R_2

$$V_o = 1.25\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2$$

$$V_o = 1.25\left(1 + \frac{R_2}{240}\right) + 100 \times 10^{-6} \times R_2$$

For V_o = 6V i.e. minimum the corresponding value of R_2 will be R_{2min}

$$\therefore 6 = 1.25\left(1 + \frac{R_2}{240}\right) + 10^{-4} \times R_2$$

R_{2min} = 894.48 Ω

For V_o = 12V , value of R_{2max} will be

$$\therefore 12 = 1.25\left(1 + \frac{R_2}{240}\right) + 10^{-4} \times R_2$$

R_{2max} = 2025.24 Ω

Thus we want R_2 to vary from 894.48 Ω to 2025.24 Ω. Hence we choose R_2 to be a series combination of a fixed resistor of 680 Ω and a potentiometer of 1k Ω value.

2. To obtain 500mA, we should use TO-3 package with 20W power consumption rating.

3. Filter capacitors:

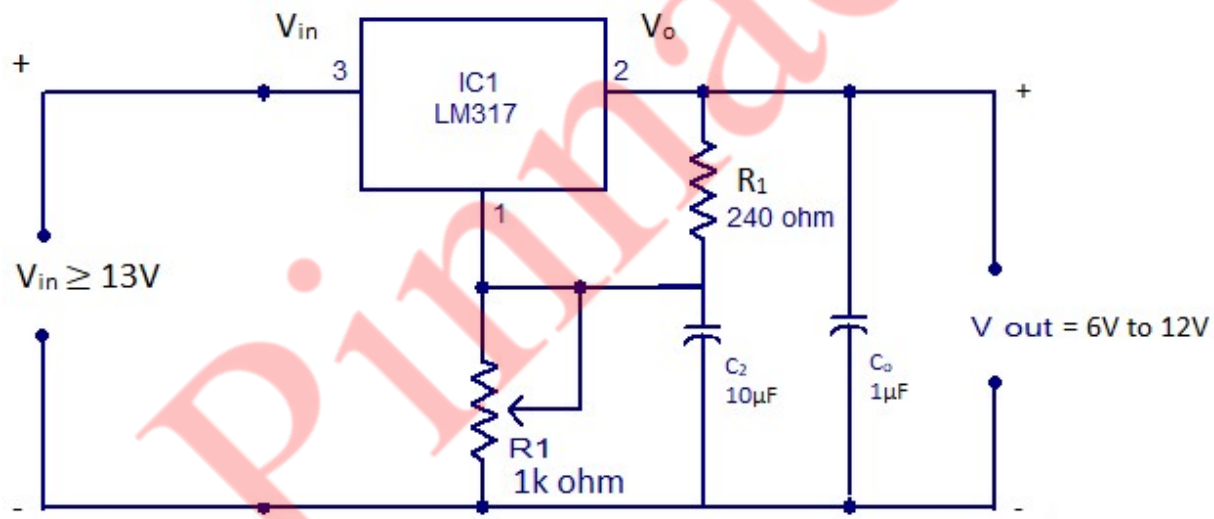
We assume that the regulator is close to the unregulated input supply. Hence the input capacitor C_i is not to be used. But for better ripple rejection use capacitor C_2 = 10µF between adjustment terminal and ground. The output capacitor C_o=1 µF is also being used.

4. Protective diodes:

As the output voltage is less than 25V and capacitors are smaller than 25µF, it is not necessary to use the protective diodes.

The minimum voltage drop across LM 317 is 3V. Hence the input voltage $V_{in} \geq 13V$.

Hence the complete designed Voltage regulator is as shown below:



Q.5.

a) Design a Wein bridge oscillator using op-amp to oscillate a frequency of 965 Hz and explain the working of Wein bridge oscillator. (10)

SOLUTION:

f_o = 965 Hz

Let us assume C= 0.01 µF = 0.01 ×10^{-6} F.

To calculate value of R, R_1 and R_F:

$f_o = \frac{1}{2\pi R}$

$\therefore R = \frac{1}{2\pi fo} = \frac{1}{2\times3.142\times965\times0.01\times10^{-6}}$

R = 16.49kΩ.

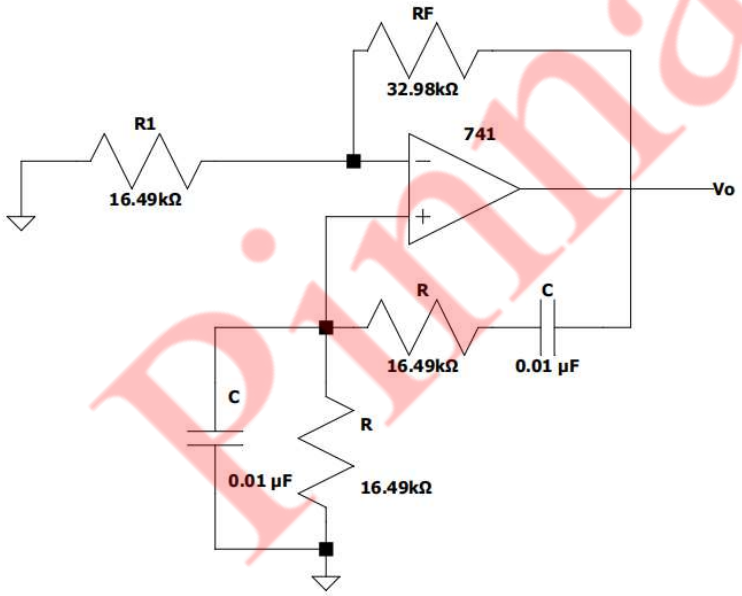
Let R_1=R

R_1=16.49kΩ

$R_F \geq 2R_1$

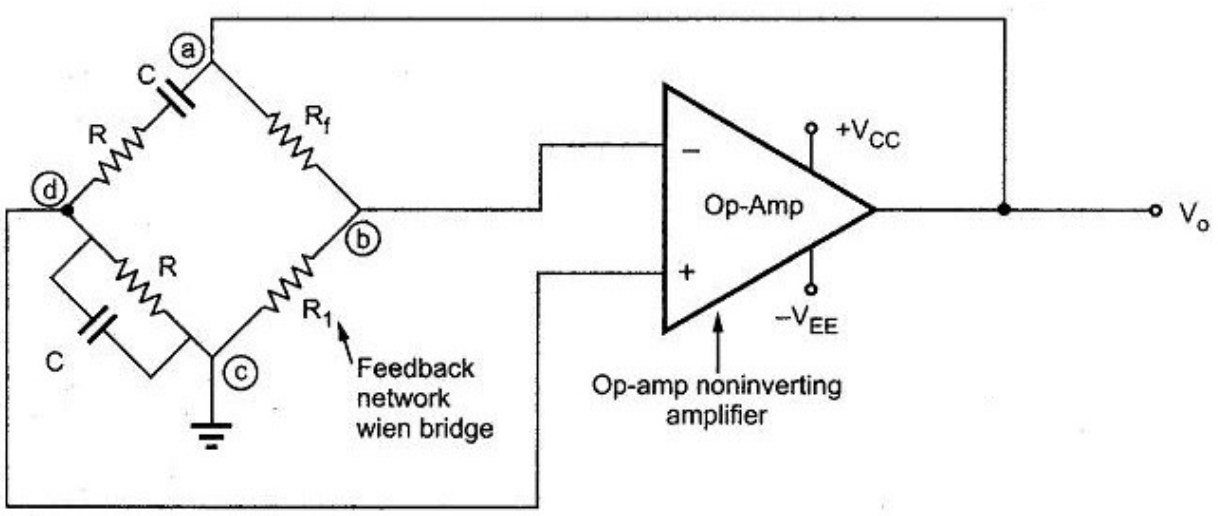
R_F=32.98 kΩ

The designed Wein bridge oscillator is as follows:



Working of Wein bridge oscillator

1. A wein bridge oscillator with a non-inverting op-amp amplifier is as shown below



2. The Wein bridge has 4 arms. The arm AD which contains a series of combination of R and C, whereas arm CD contains a parallel combination of R and C.

This value of R and C is used to decide the value of oscillator frequency such that

$$f = \frac{1}{2\pi RC}$$

3. The resistors R_F and R_1 are used to generate a reference voltage which remains constant independent of the frequency f.

4. The AC input voltage is applied between the points A and C of the bridge. When Wein bridge is used in oscillator circuit, the feedback voltage is applied between these points.

5. The AC output of the bridge is obtained between the points B and D which is connected as inputs of the non-inverting amplifier.

6. The value of feedback factor β depends upon the frequency. At oscillator frequency f_o the phase shift introduced is zero and thus value of feedback factor β is 1/3.

7. According to Barkhausen criteria the phase shift around the loop should be zero and loop gain should be greater than 1.

i.e. $|A\beta| \geq 1$

substituting $\beta = 1/3$, we get $A \geq 3$.

Therefore the gain of the amplifier should be greater than or equal to 3.

b) List and explain the various performance parameters of DAC. (10)

SOLUTION:

1. Resolution:

- Resolution is defined as the smallest possible change in the analog output voltage. Resolution should be as high as possible.
- Resolution depends upon the number of bits in digital input applied to DAC such that Resolution=2^n for n bits.
  Therefore, Resolution increases with increase in number of bits.
- If V_{FS} is the full scale analog output voltage then resolution of DAC is
  Resolution = $\frac{V_{FS}}{2^n-1}$

2. Accuracy:

- Accuracy of a DAC indicates how close the analog output voltage is to theoretical value or simply the deviation of actual output from theoretical value.
- Accuracy depends upon the accuracy of the values of resistors used in the ladder and the precision of the reference voltage used.
- Accuracy is always specified in terms of percentage of the full scale output. That means maximum output voltage eg. If the full scale output is 15V and accuracy is ±0.1% then the maximum error is given by 0.001 × 15= 0.015 V or 15mV.

3. Linearity:

- The relationship between the digital input and analog output is expected to be linear. However practically it is not so due to error in the values of resistor used for the resistive network.

4. Temperature Sensitivity:

- The ideal requirement is that analog output voltage of DAC should not change due to changes in temperature. But practically analog output is a function of temperature. It is so because the resistance values and op-amp parameters change with changes in temperature.

5. Setting time:

- Theoretically the analog output voltage should change instantaneously as soon as there is a change in the digital input.
- Practically the analog output of DAC does not change instantaneously. Due

to resistors and op-amp in the circuits, oscillations are observed at the output.

- The time required to settle the analog output within ½ LSB of the final value, from the instant of change in digital input is called as setting time.

- The setting time should be as small as possible.

6. Speed:

- It is defined as the time taken by a DAC to perform a conversion from digital to analog.
- It is also defined as the number of conversions that can be performed per second.
- Speed of a DAC should be as high as possible.

7. Long term drift:

- This results mainly due to resistor and semiconductor aging and can affect all the characteristics. Characteristics mainly affected are speed, linearity, etc.

8. Supply rejection:

- It indicates the ability of DAC to maintain all its important characteristics unchanged when the supply voltage is varied. Supply rejection is usually specified as percentage of full scale change at or near full scale at 25˚C.

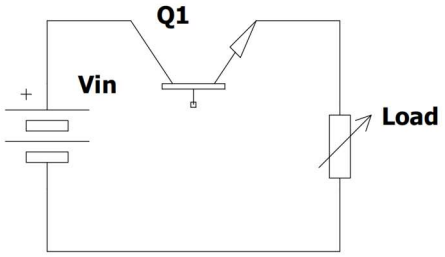
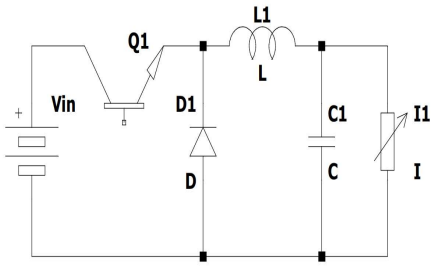
9. Input-Output Equation:

- The input output equation of a DAC can be used to calculate the analog output voltage corresponding to given digital input word.
- The output voltage (V_o) equation can be given as
  $V_o = K V_R D$
  Where D is fractional binary value and is given as
  $D = (d_1 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n})$
  Where d_1 is MSB and d_n is LSB.
- Or V_o can be simply given as
  V_o = Resolution × D.

Q.6. Short notes on (Attempt any 4): (20)

a) Comparison of linear and switching regulators.

SOLUTION:

Sr.No.	Parameter	Linear Regulator	Switching Regulator
1	Circuit Diagram		
2	Region of operation	Active region	Saturated or Cut-off
3	Switching	No switching	Transistor acts as a switch
4	Complexity	Less	High
5	Efficiency	Low (40%)	High (90%)
6	Switching frequency	Very low	Very high (25kHz)
7	Switching losses	Zero	Very high
8	RFI/EMI	Absent	Very high
9	Component stress	High	Very high
10	Regulation	Excellent	Good
11	Cost	Lowest	Moderate
12	Size/Weight	Large/Bulky	Small/Light weight
13	Power handling capacity	Low	High

b) Active filters using opamp:

SOLUTION:

1. Active filters use active devices like op-amp and transistor along with the passive components like resistor, capacitor or inductors.

2. An active low pass filter designed using op-amp can be shown as below

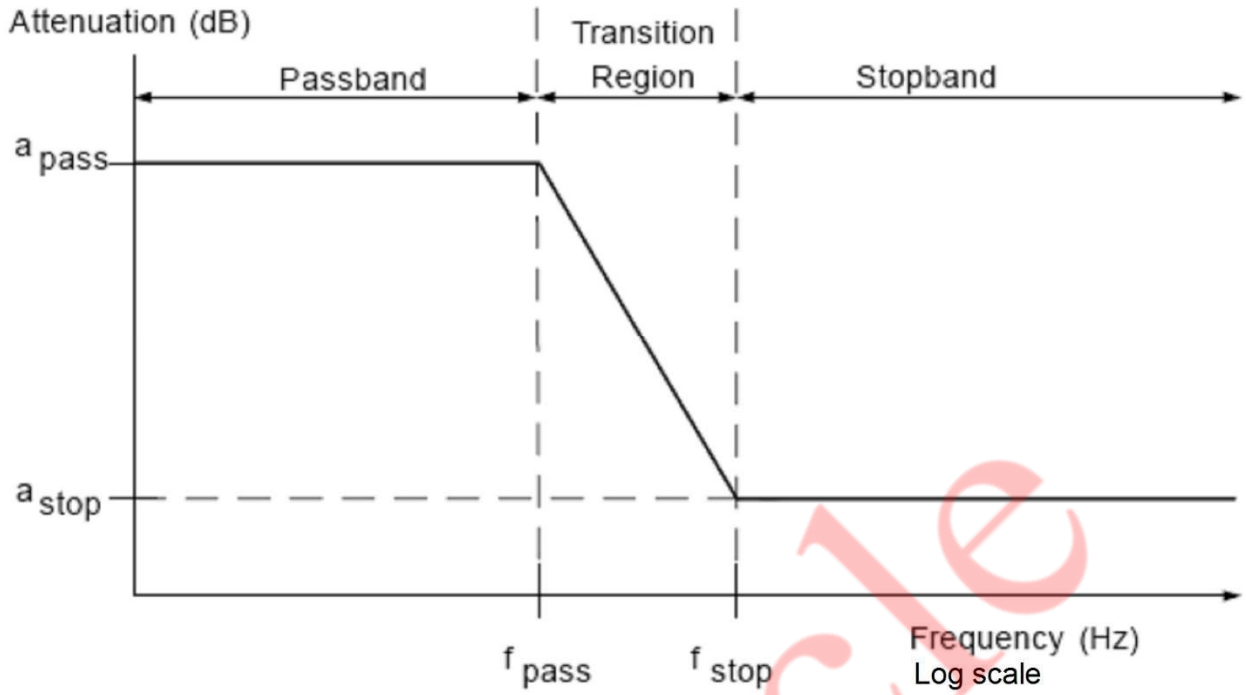
3. The RC circuit together forms a passive low pass filter since they are passive elements.

4. The input V_{in} is applied to this RC circuit and the output V_o is applied back to input of the amplifier.

5. In active filter op-amp is used as a non-inverting amplifier where R_F and R_1 can be selected for desired value of passband gain such that

$$A_{VF} = 1 + \frac{R_F}{R_1}$$

6. The frequency response of an active low pass filter can be given as



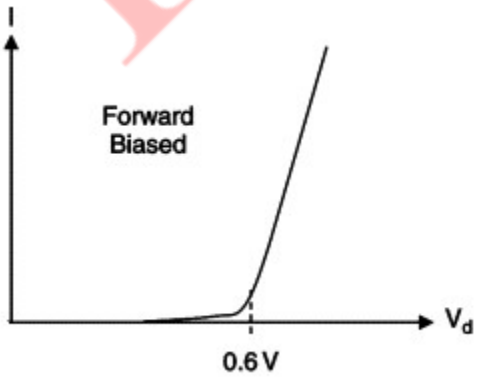
Features:

- It is possible to provide desired gain.
- The frequency response becomes more sharp.
- The passband and stopband can be separated clearly.

c) Precision Rectifiers:

SOLUTION:

1. In conventional rectifier circuits it is not possible to rectify AC voltages below 0.6 volts, because the minimum voltage required to forward bias a silicon diode is 0.6 volts as shown in graph below of forward characteristics of silicon diode



2. By using precision rectifiers it is possible to rectify the AC input voltages of very small magnitudes even less than0.6 volts.

3. The distortion in precision rectifiers is reduced as compared to conventional rectifiers. Also the transfer characteristics is linear.

4. Precision rectifiers have high impedance hence loading on the input source is reduced.

5. There are two main classification of precision rectifier:

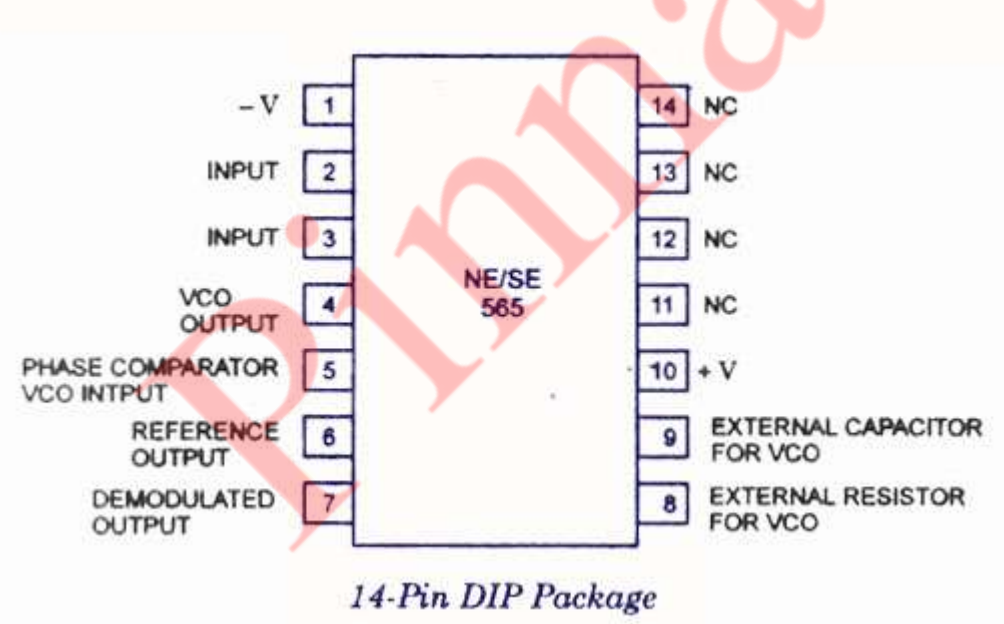
- Precision half wave rectifier (HWR)
- Precision full wave rectifier (FWR)

Precision half wave rectifier can be implemented using inverting and non-inverting amplifier as well.

d) PLL IC 565:

SOLUTION:

1. PLL IC 565 is a 14 pin DIP and 10 pin metal can package. Pin configuration of 565 is as shown below



14-Pin DIP Package

2. Functional block diagram of IC 565 is as shown below

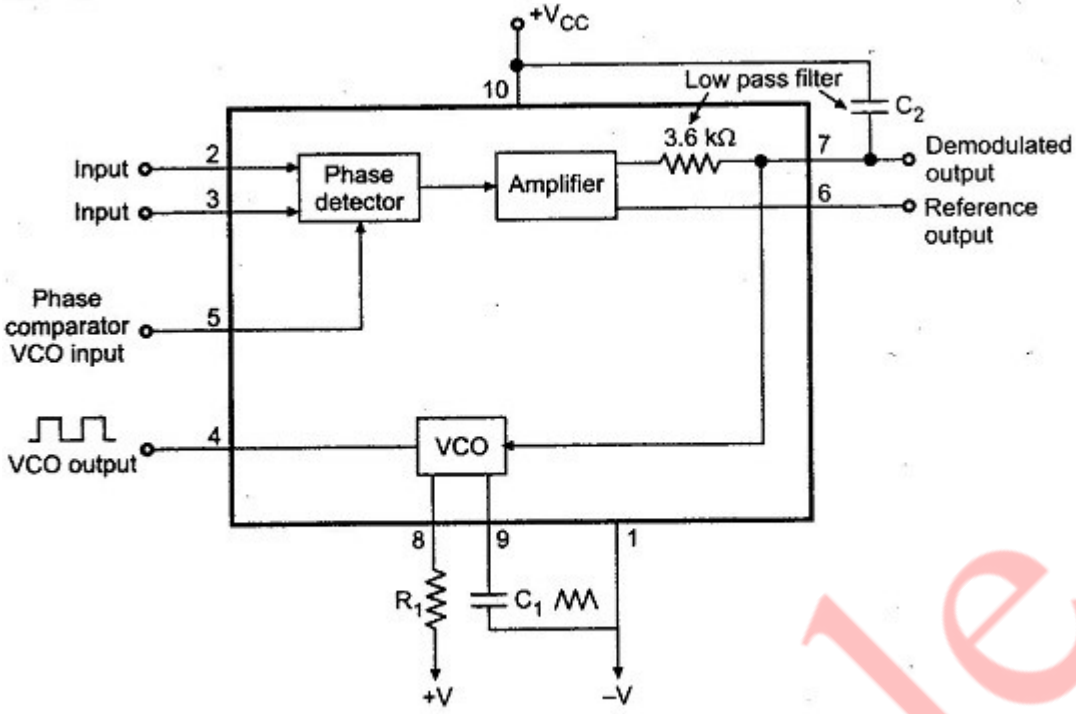


Fig. 2.125 Block diagram of IC 565 PLL

3. The free running frequency of VCO (i.e. when inputs 2 and 3 are grounded) is given by

$$f_o = \frac{0.3}{R_T C_T}\ Hz$$

Where R_T and C_T are externally connected components to pin 8 or pin 9 respectively as shown in functional block diagram.

This externally connected R_T can have a value between 2kΩ and 20kΩ whereas C_T can have any value.

4. To compare f_i and f_o pin 4 and pin 5 is connected externally.

5. The 3.6kΩ external resistor along with capacitor C connected between pin 7 and pin 10, such that value of this capacitor C should be sufficiently large to minimize variation in output at pin 7.

6. The 565 PLL is capable of locking to and tracking an input signal over ±60% bandwidth with respect to f_o (center frequency).

7. The lock range f_L of the PLL is given by

Lock range: $\Delta f_L = \pm \frac{8\, f_o}{V}\ Hz$

Where f_0= free running frequency of VCO in Hz

V=(+V) - (-V) volts.

8. The expression for the capture range is given by:

Capture range : $\Delta f_c = \pm \left(\frac{\Delta f_l}{(2\pi)(3.6)\times 10^3 \times C} \right)^{1/2}$

Where C is expressed in farads.

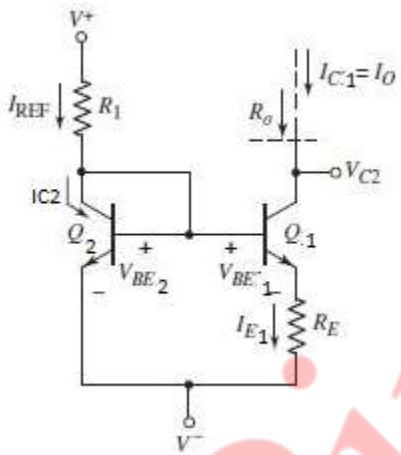
e) Widlar current source:

SOLUTION:

1. In other current sources the output current I_o is approximately equal to reference current I_{REF}. To avoid this condition value of R should be as large as 1MΩ which is not possible to implement in an IC.

Therefore Widlar current source is used.

2. Widlar current source using transistors is represented as follows



Such that

- Both Q_1 and Q_2 are identical.
- β of both the transistors is large.

3. Due to voltage drop at R_E the V_{BE1} of Q_1 will always be less than V_{BE2} of transistor Q_2.

∴ $V_{BE1} = V_{BE2}$.

4. As V_{BE1} is small, the value of I_{C1} will also be smaller which means that the output (load) current I_o will be smaller than I_{REF}.

∴ $I_o < I_{REF}$.

Thus $I_{B1} \neq I_{B2}$ and $I_{C1} \neq I_{C2}$ for Widlar current source.

5.Due to this asymmetric arrangement and nature of base and collector; V_{CC} ,Q_2 and R_1 will establish a reference current I_{REF} and then R_E will determine difference between I_{C1} and I_{REF}.

6. Output resistance R_o at Q_1 is given by

$R_o \approx r_{01}(1 + g_{m1}R_E)$.

7. Advantages of Widlar current source:

- Smaller value of R_1 for small values of I_o therefore the fabrication of R_1 on IC chip becomes possible.
- Improved stability of I_o against variation in V_{CE} of output transistor.
- High output resistance.